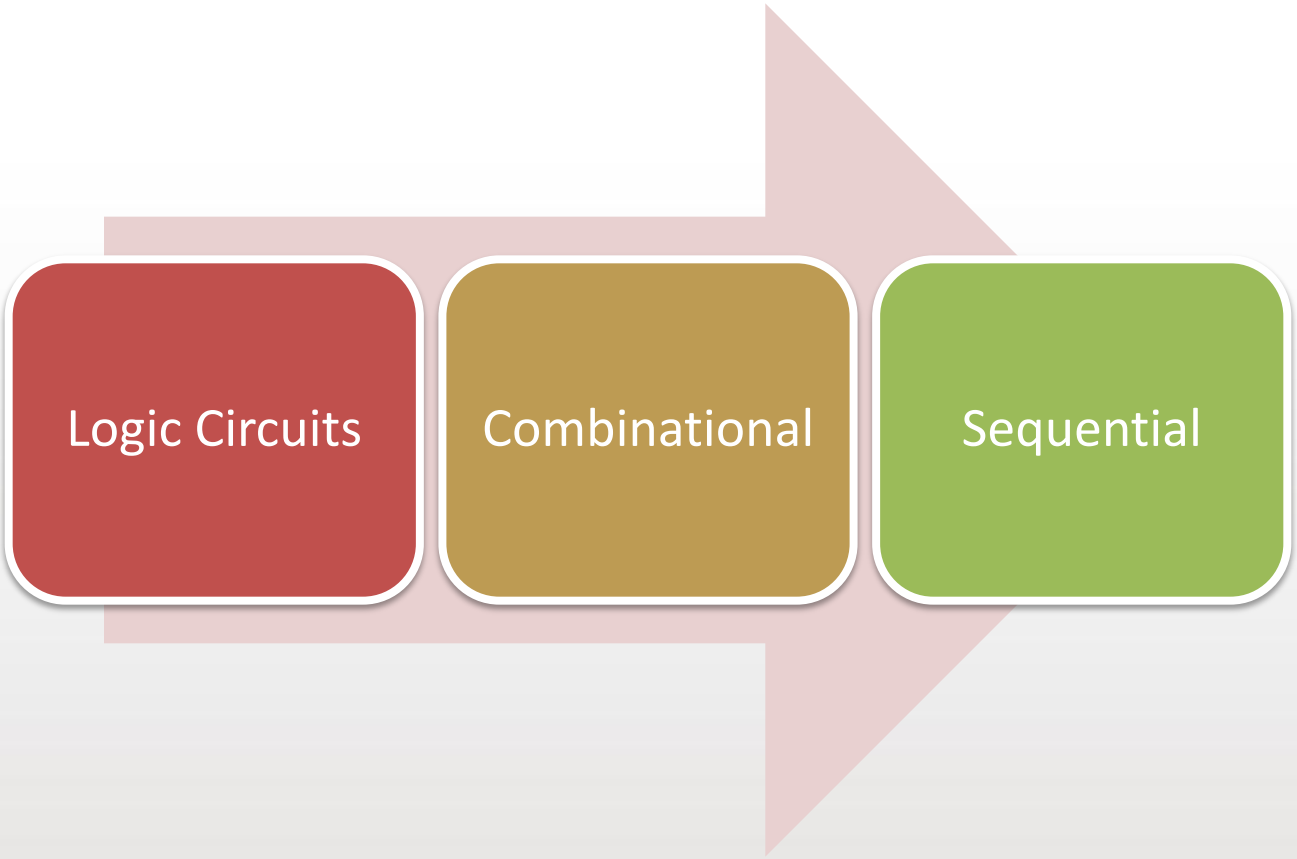
Digital Electronics (SKEE1223)

Latches & Flip-Flops

Muhammad Arif Abd Rahim
Muhammad Mun'ím Ahmad Zabidi
Ab Hadi Abd Rahman

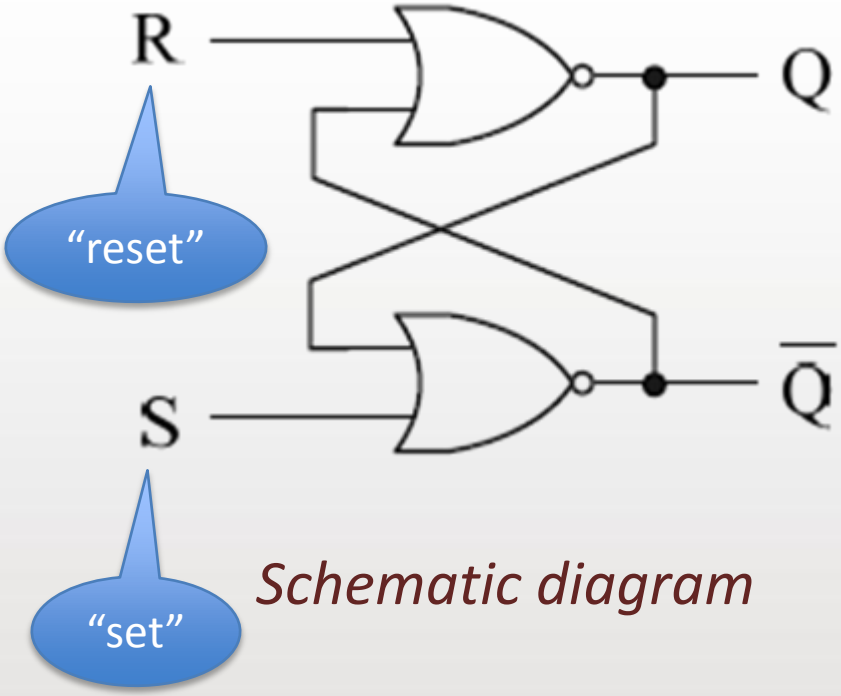
Faculty of Electrical Engineering


Logic Circuits
Combinational
Sequential

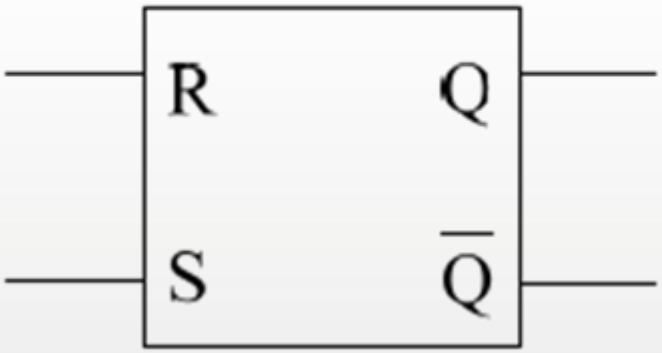
Logic Circuits

	Combinational	Sequential
Characteristic	Output depends only on present inputs	Output depends on present and past inputs
Example devices	Gates, decoders, multiplexers, adders	Latches, flip-flops, registers, counters, processors

SR Latch



Schematic diagram



Logic diagram

SR Latch

Present State

Next State

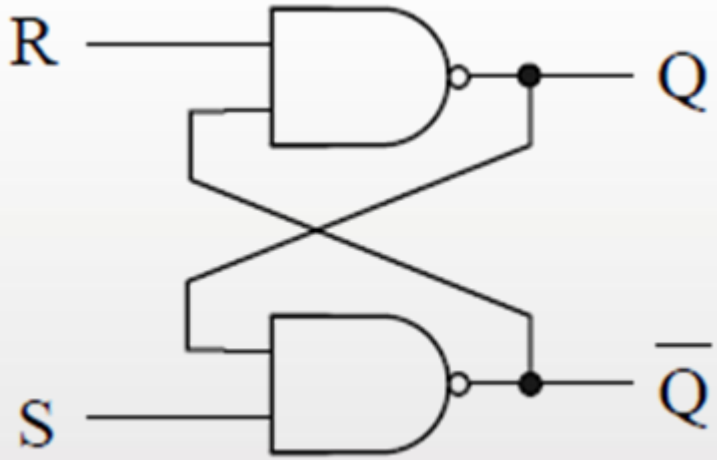
R	S	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	Illegal inputs
1	1	1	Illegal inputs

Truth table

R	S	Q_{n+1}
0	0	Q_n(no change)
0	1	1 (set)
1	0	0 (reset)
1	1	Illegal inputs

Simplified truth table

NAND Version

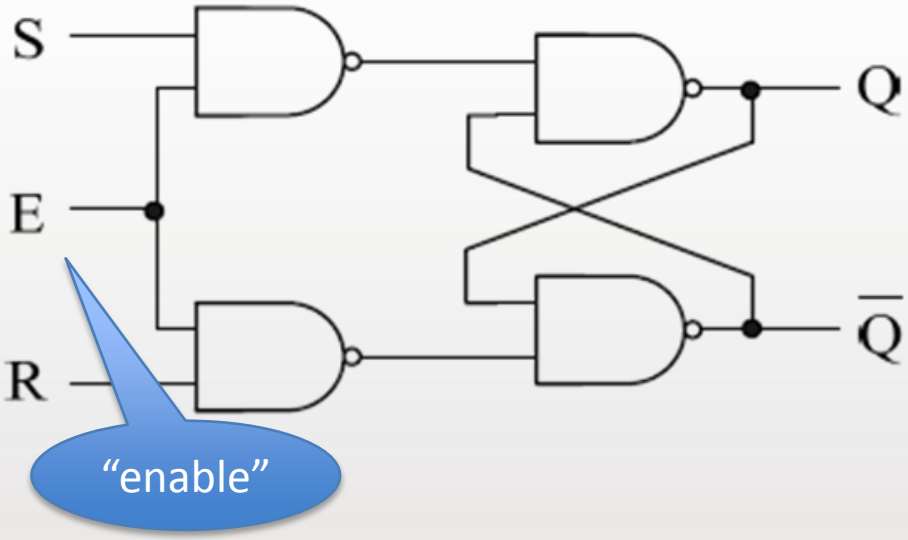


Schematic diagram

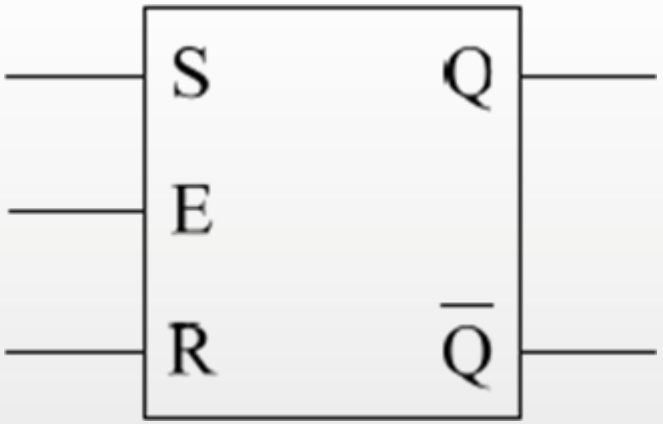
R	S	Q_{n+1}
0	0	Illegal inputs
0	1	1
1	0	0
1	1	Q_n

Simplified truth table

Gated SR Latch



Schematic diagram

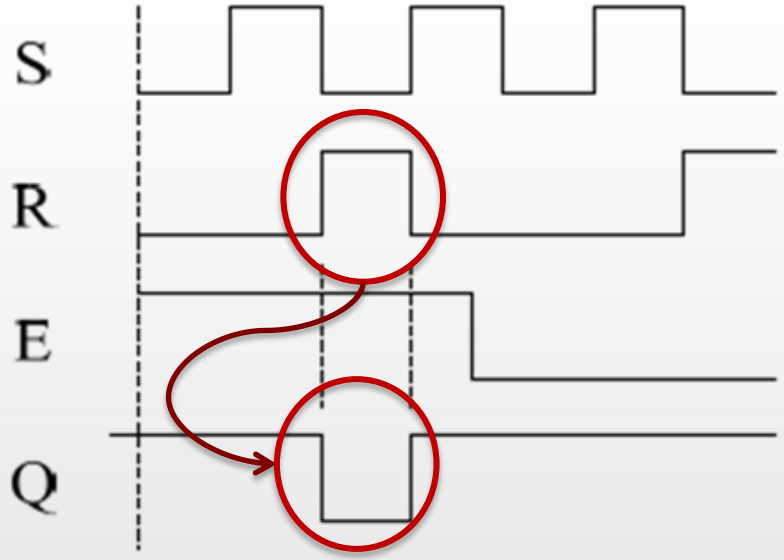


Logic symbol

Gated SR Latch

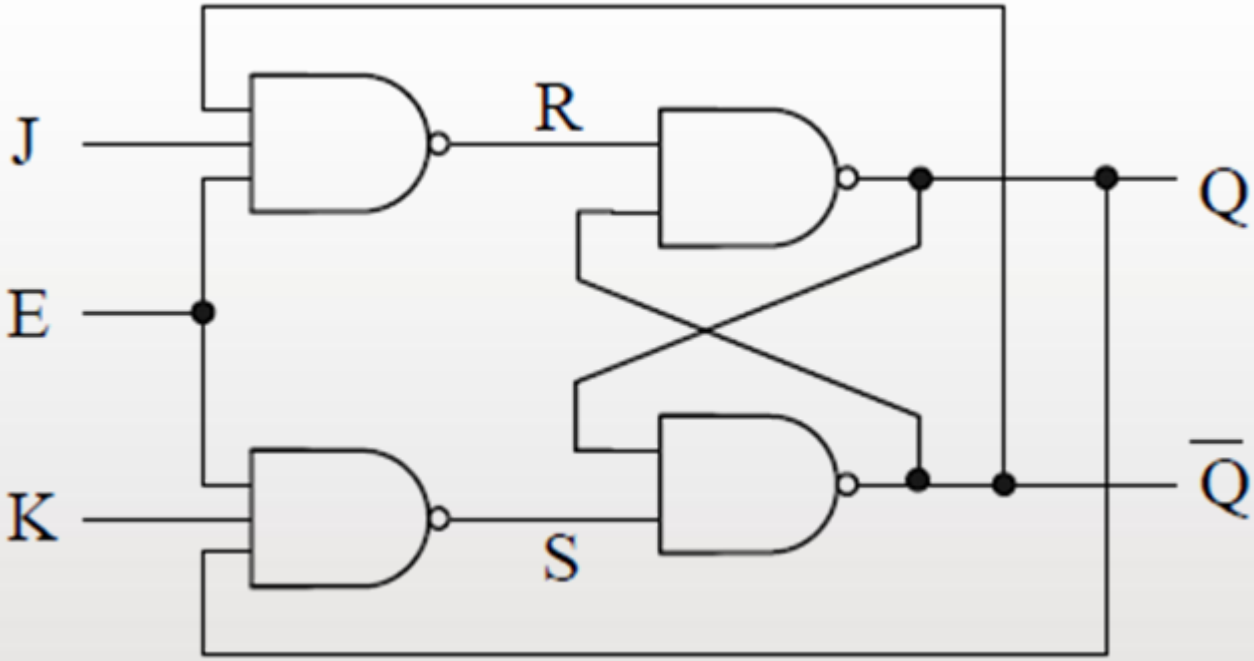
E	R	S	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Illegal inputs

Truth table



Timing diagram

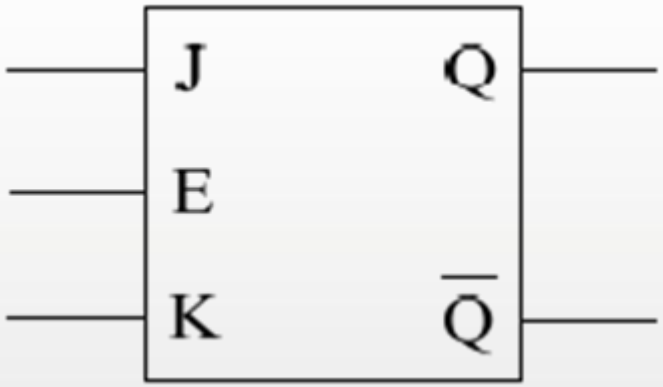
Gated JK Latch



Gated JK Latch

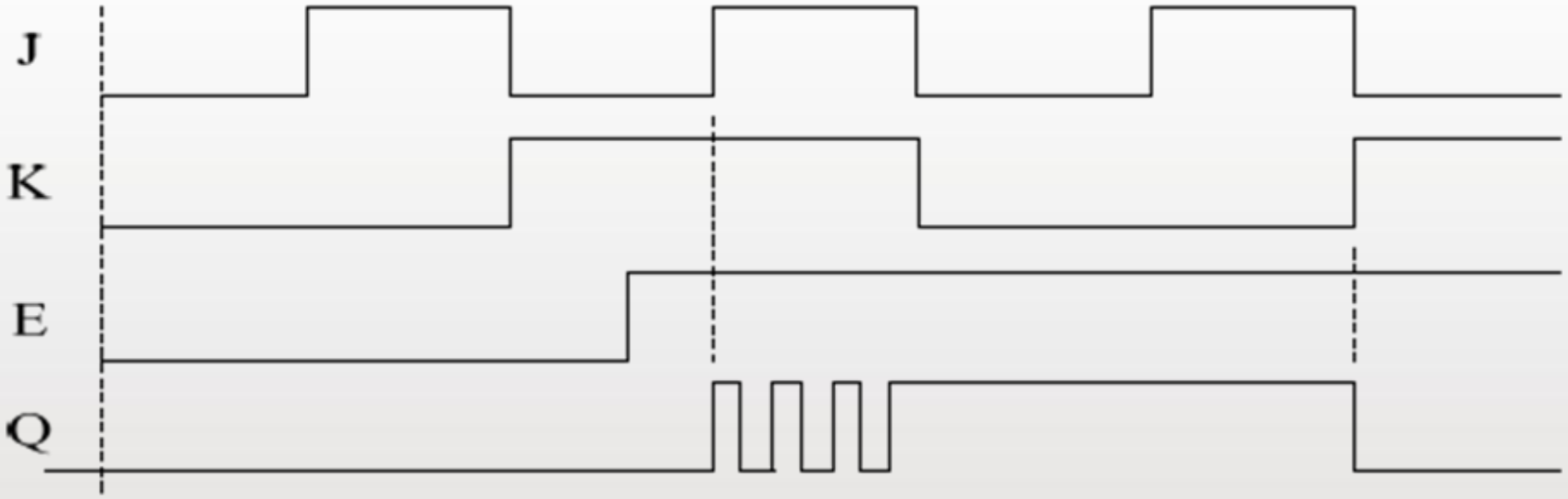
E	J	K	Q_{n+1}
0	X	X	Q_n (no change)
1	0	0	Q_n (no change)
1	0	1	0 (reset)
1	1	0	1 (set)
1	1	1	$\overline{Q}_n$ (toggle)

Truth table.

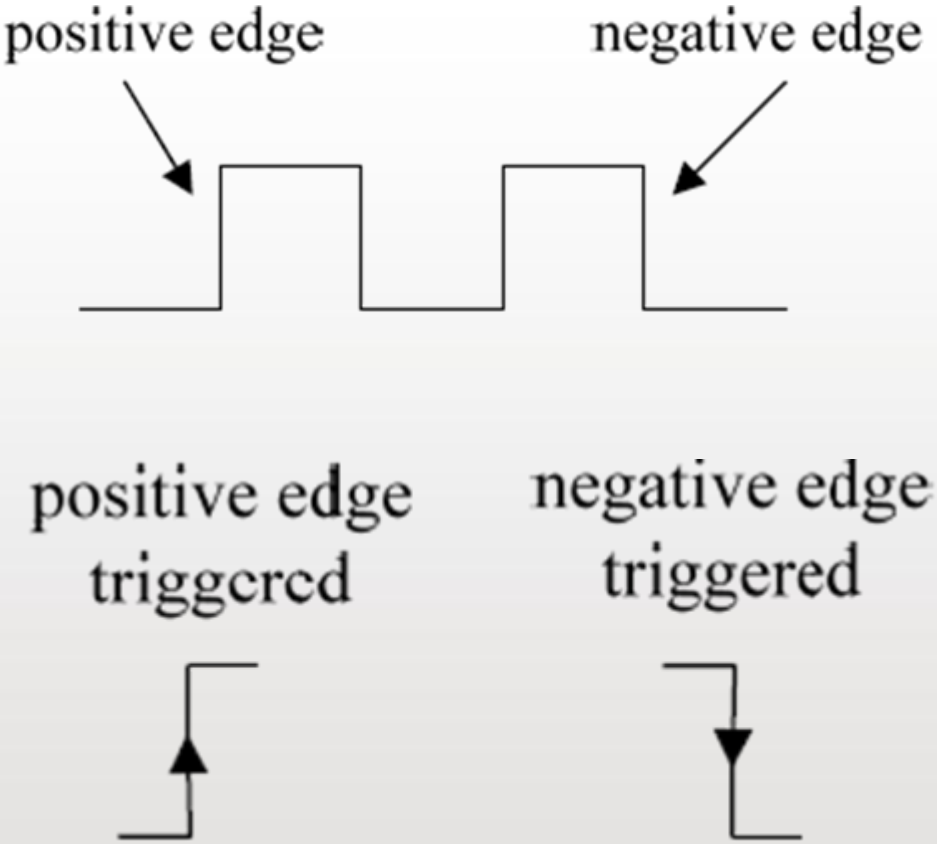


Logic symbol.

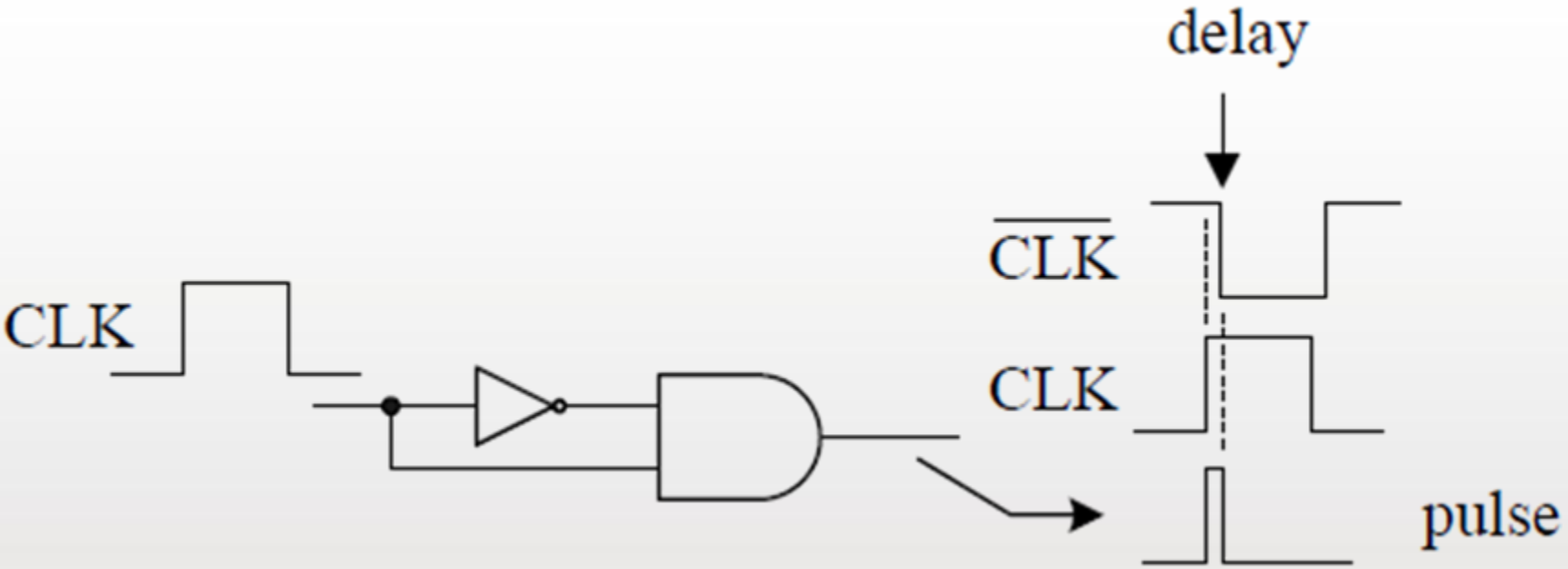
Level Triggered JK Latch



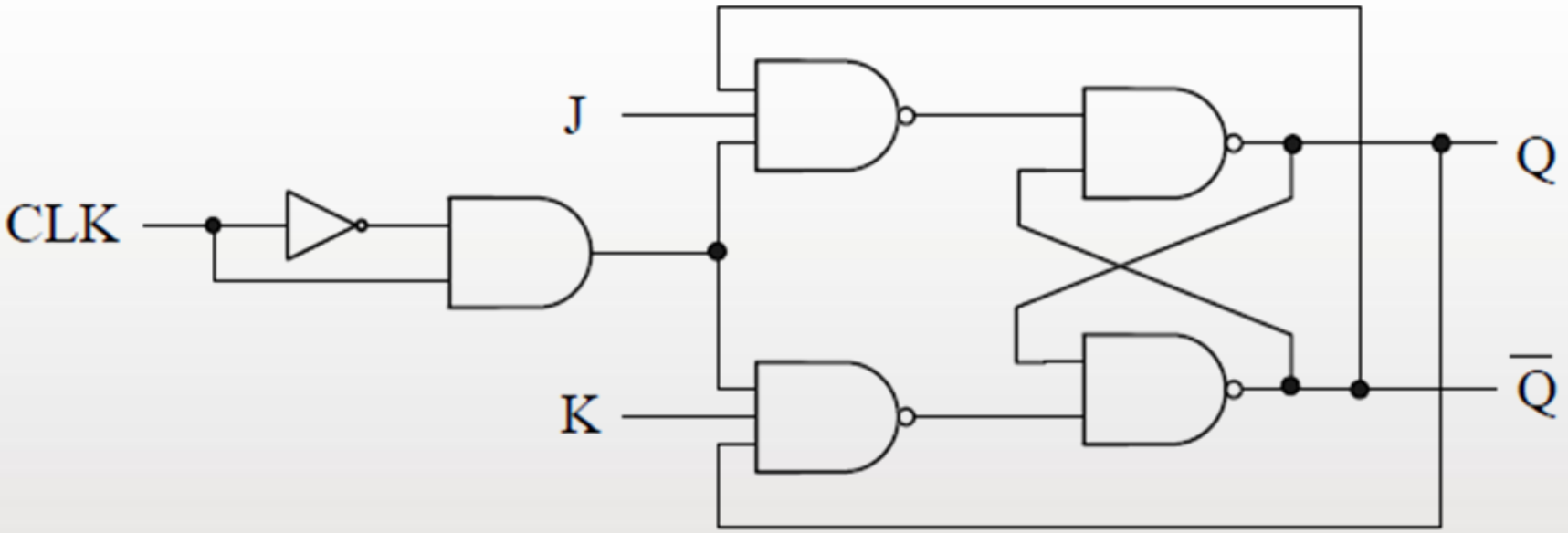
Clocks


positive edge
negative edge
positive edge triggered
negative edge triggered

Narrow Pulse Generation



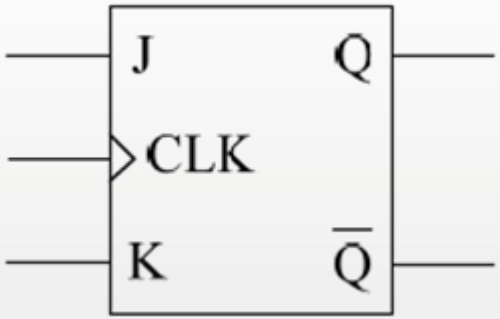
Positive Edge Triggered JK Flip-Flop



JK Flip-Flop

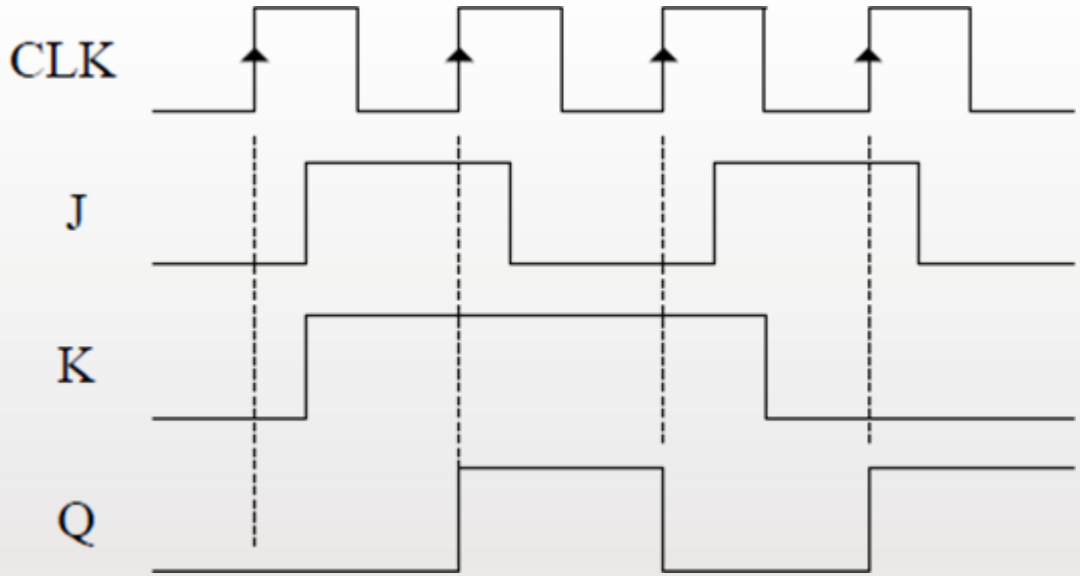
CLK	J	K	Q_{n+1}
↓	X	X	Q_n
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	$\overline{Q_n}$

Truth table



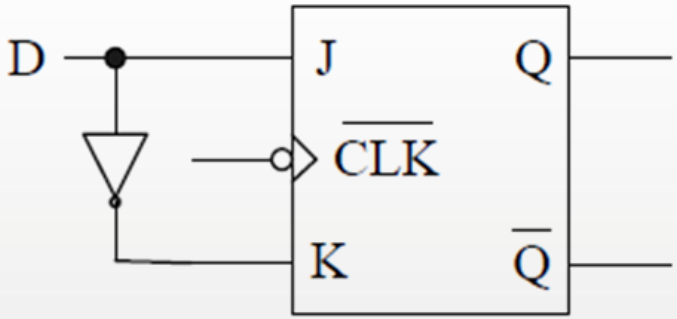
Logic symbol

JK Flip-Flop Timing Diagram

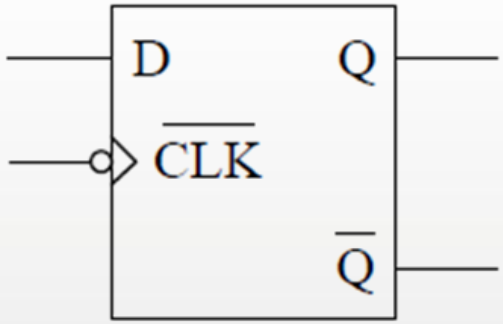


Negative Edge Triggered D Flip-Flop

Implemented using JKFF



Logic symbol

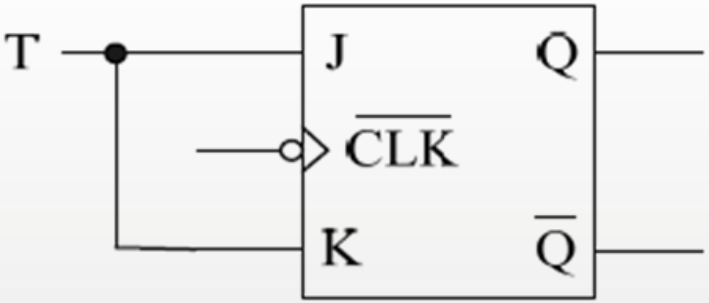


$\overline{CLK}$	D	Q_{n+1}
↑	X	Q_n
↓	0	0
↓	1	1

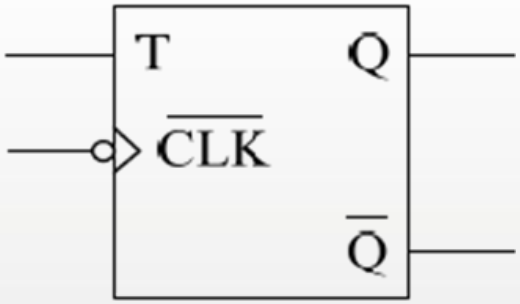
Truth table

Negative Edge Triggered T Flip-Flop

Implemented using JKFF



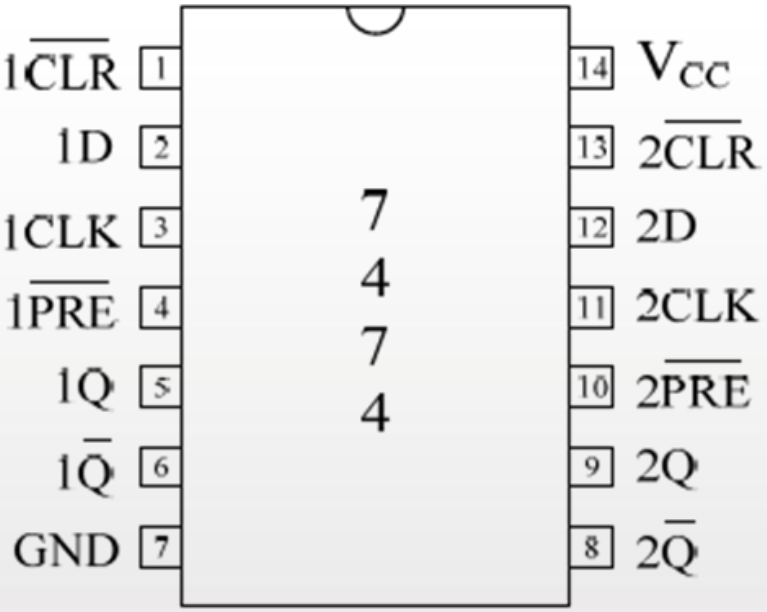
Logic symbol



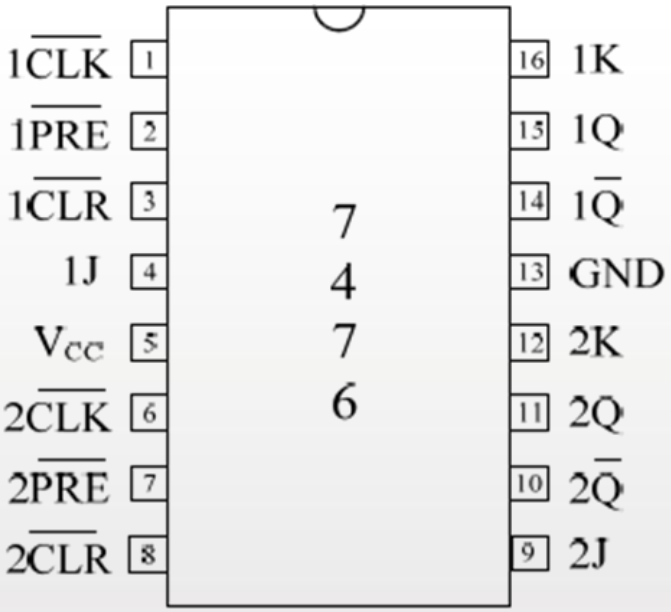
$\overline{CLK}$	T	Q_{n+1}
↑	X	Q_n
↓	0	Q_n
↓	1	$\overline{Q_n}$

Truth table

Flip-Flop Chips

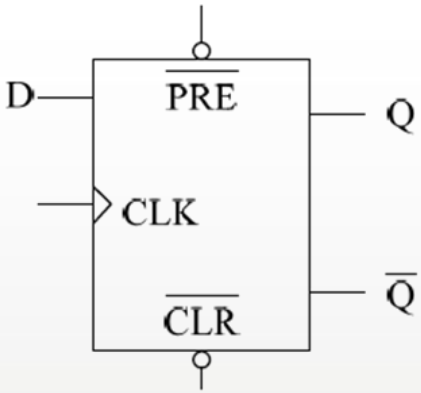


7474 D Flip-Flop

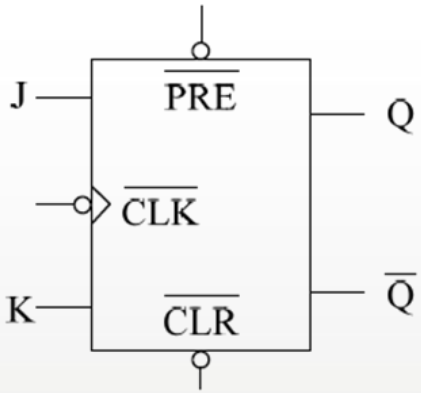


7476 JK Flip-Flop

Preset and Clear Functions



7474



7476

$\overline{PRE}$	$\overline{CLR}$	Operation
0	0	Not used
0	1	Set (Q = 1)
1	0	Clear (Q = 0)
1	1	Flip-flop operation

Truth table.

7476 Timing Diagram