SEE1223: Digital Electronics

5 – Latches and Flip-Flops

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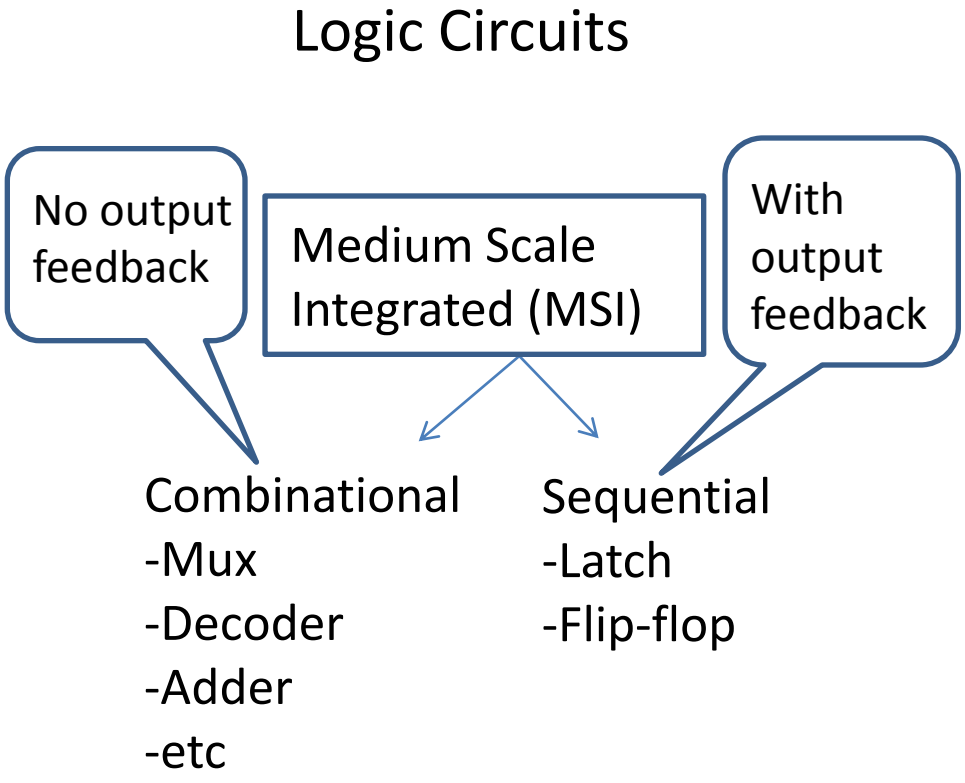
Latches and Flip-Flops

- Introduction to sequential logic
- Latches
  - SR Latch
  - Gated SR Latch
  - Gated D Latch
- Flip-Flops
  - JK Flip-flop
  - D Flip-flop
  - T Flip-flop
  - JK Master-Slave Flip-flop
  - Preset and Clear functions
  - 7474 and 7476 devices

Sequential vs Combinational Logic

- Digital circuits can be categorized into combinational or sequential logic



Latch

- Latch is a type of temporary storage device, where the output feeds back to the input
- It is a basic form of memory, i.e. we can store a value of ‘1’ or ‘0’ in a latch
- Latches however, are considered unstable in modern circuits and rarely used, but crucial in understanding flip-flops
- Flip-flops are the dominant sequential circuit element, and are present in almost all digital systems

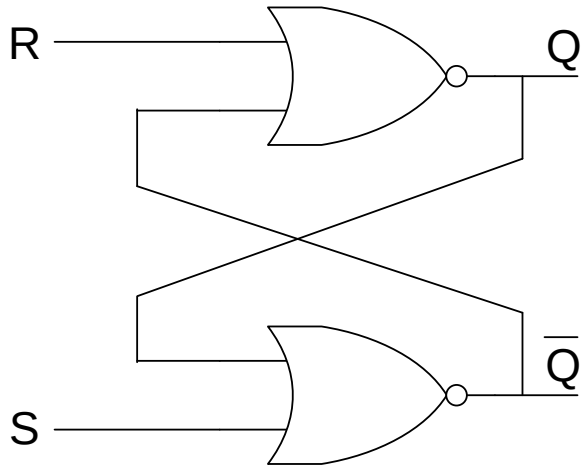
SR Latch

- The SR latch (Set-Reset latch) is the most basic type, which can be constructed using NOR or NAND gates
- NOR gate SR latch is an active high input SR latch
- NAND gate SR latch is an active low input SR latch

SR Latch (cont.)

- Active High input SR Latch using NOR gates

Logic circuit



Truth table

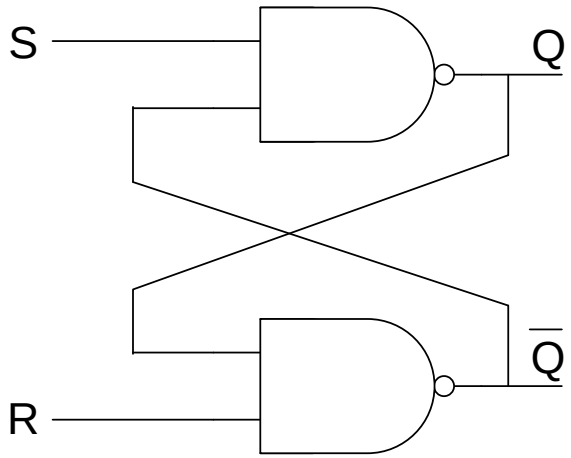
S R	Q	$\overline{Q}$
0 0	No change	No change
0 1	0	1
1 0	1	0
1 1	0(invalid)	0(invalid)

When R = 1 and S = 0, the latch is reset (Q = 0)
When R = 0 and S = 1, the latch is set (Q = 1)
When R = 0 and S = 0, Q and $\overline{Q}$ maintains the previous value
When R = 1 and S = 1, both Q and $\overline{Q}$ are 0, which is invalid

SR Latch (cont.)

- Active Low input SR Latch using NAND gates

Logic circuit

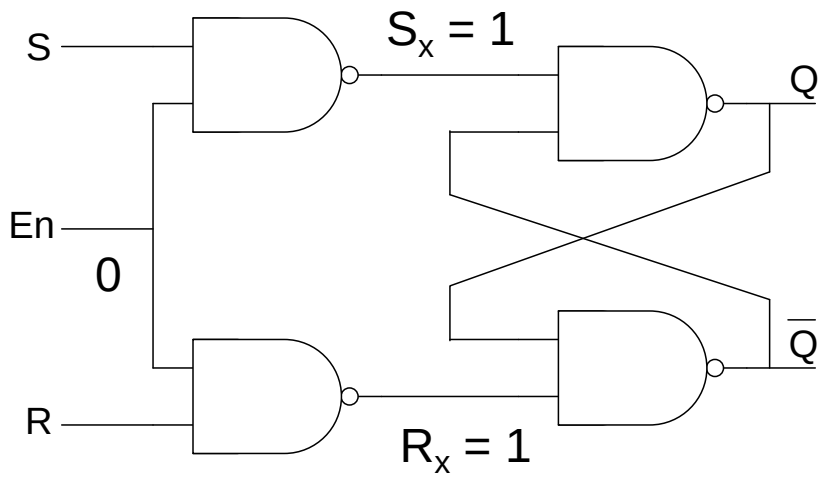


Truth table

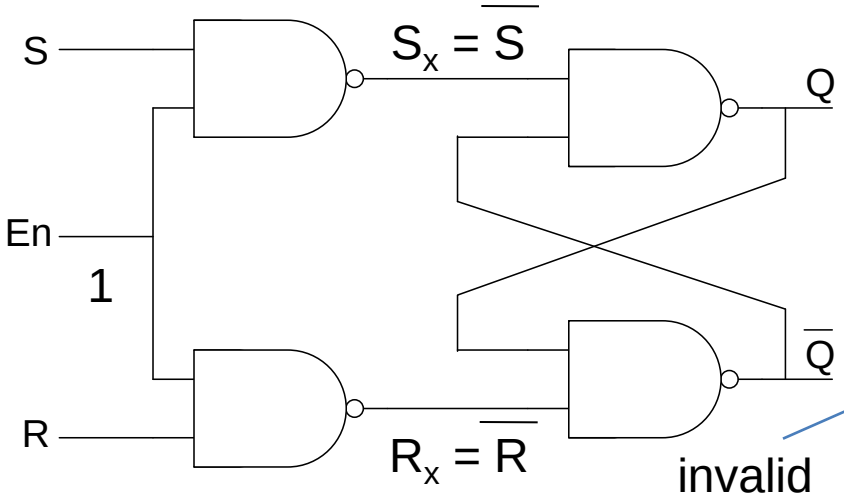
S R	Q	$\overline{Q}$
0 0	1(invalid)	1(invalid)
0 1	1	0
1 0	0	1
1 1	No Change	No Change

When R = 0 and S = 1, the latch is reset (Q = 0)
When R = 1 and S = 0, the latch is set (Q = 1)
When R = 1 and S = 1, Q and $\overline{Q}$ maintains the previous value
When R = 0 and S = 0, both Q and $\overline{Q}$ are 1, which is invalid

Gated SR Latch (active high enable)



When $\overline{En}$ = 0 (disable),
Q and $\overline{Q}$ maintains previous value,
Regardless of S and R

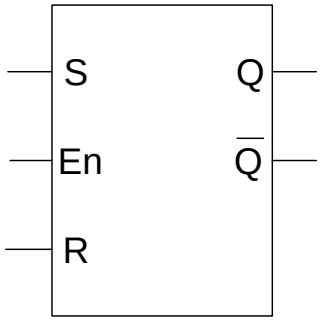


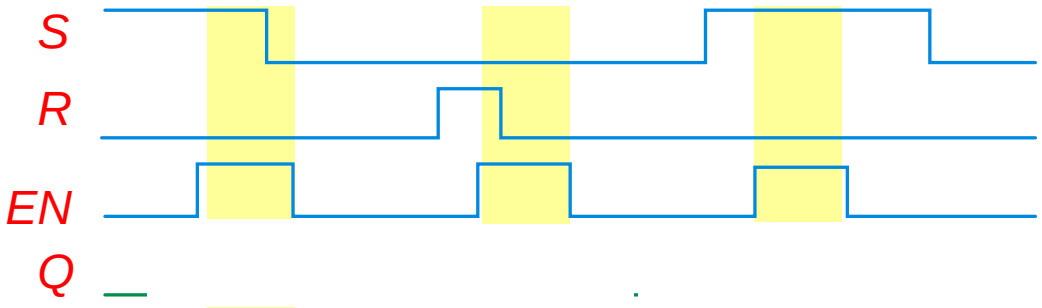
When En = 1 (enable),
The circuit becomes an active
High input SR latch

Q = 1, $\overline{Q}$ = 0 when S = 1 and R = 0
Q = 0, $\overline{Q}$ = 1 when S = 0 and R = 1
Q = $\overline{1}$, $\overline{Q}$ = 1 when S = 1 and R = 1
Q, $\overline{Q}$ maintains when S = 0 and R = 0

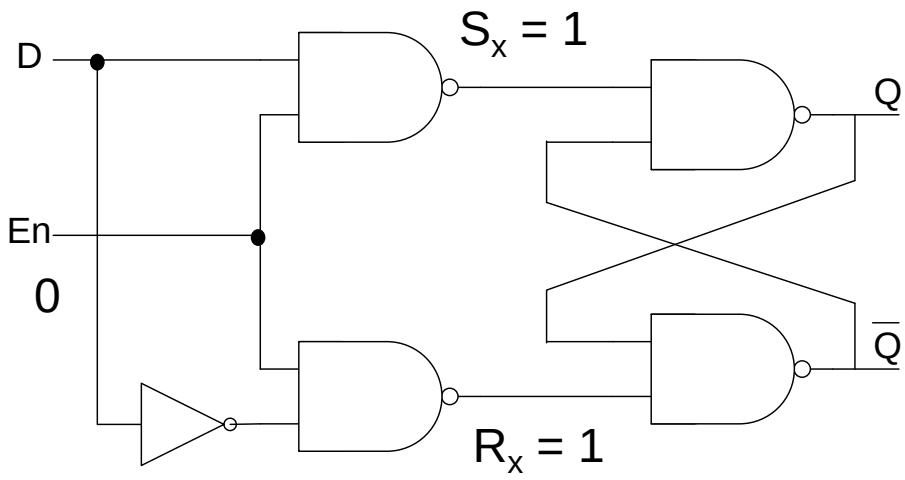
Gated SR Latch(cont.)

- Draw the output Q for the Gated SR-Latch

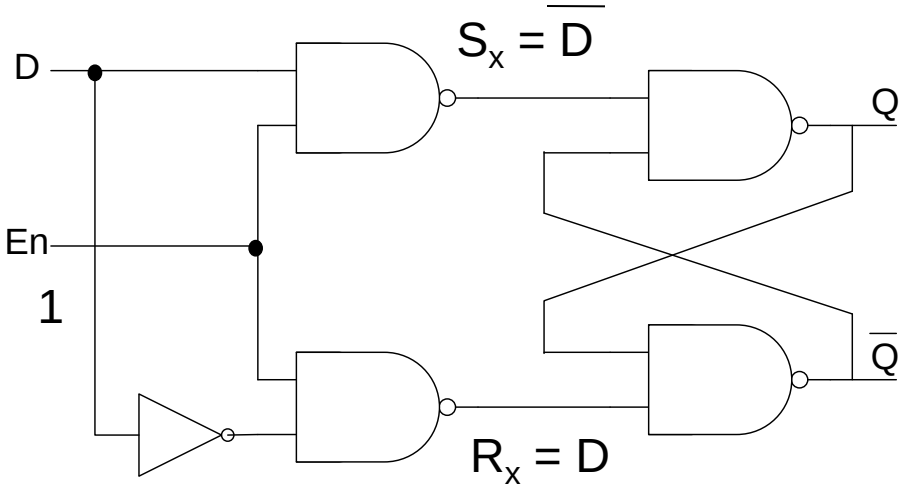




Gated D Latch (active high enable)



When $\overline{En}$ = 0 (disable),
Q and $\overline{Q}$ maintains previous value,
Regardless of D



When En = 1 (enable),

Q = 1, $\overline{Q}$ = 0 when D = 1
Q = 0, $\overline{Q}$ = 1 when D = 0

Can you derive the truth table of the Gated D-latch?

Gated D Latch (cont.)

- Draw the output Q for the Gated D Latch