Latches and Flip-Flops

- Introduction to sequential logic
- Latches
  - SR Latch
  - Gated SR Latch
  - Gated D Latch
- Flip-Flops
  - JK Flip-flop
  - D Flip-flop
  - T Flip-flop
  - JK Master-Slave Flip-flop
  - Preset and Clear functions
  - 7474 and 7476 devices

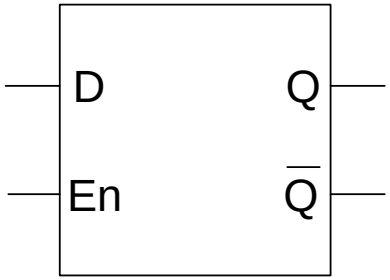
Flip-Flop

- Mostly used sequential circuit blocks for temporary storage (memory)
- For Flip-flops, output changes state only at a specified triggering input called clock (clk)
- For a latch, output changes state at a specified trigger level (high or low)

Flip-Flop (cont.)

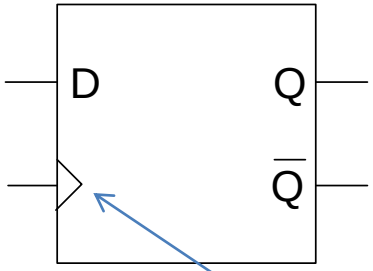
- D Latch vs D Flip Flop

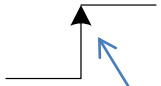
Positive level triggered D Latch/
Gated D Latch



D	En	Q	$\overline{Q}$
0	1	0	1
1	1	1	0
x	0	Q	Q

Positive edge triggered D Flip-flop





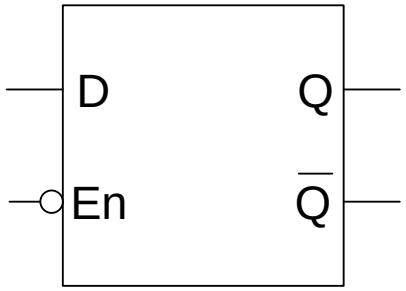
Positive edge triggered

Symbol for "clk"

D	clk	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0
x	↓	Q	$\overline{Q}$
x	0	Q	$\overline{Q}$
x	1	Q	$\overline{Q}$

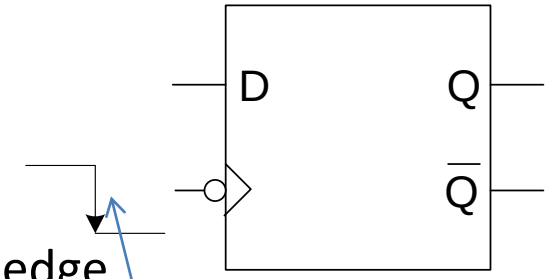
Flip-Flop (cont.)

Negative level triggered D Latch



D	En	Q	$\overline{Q}$
0	0	0	1
1	0	1	0
x	1	Q	$\overline{Q}$

Negative edge triggered D Flip-flop

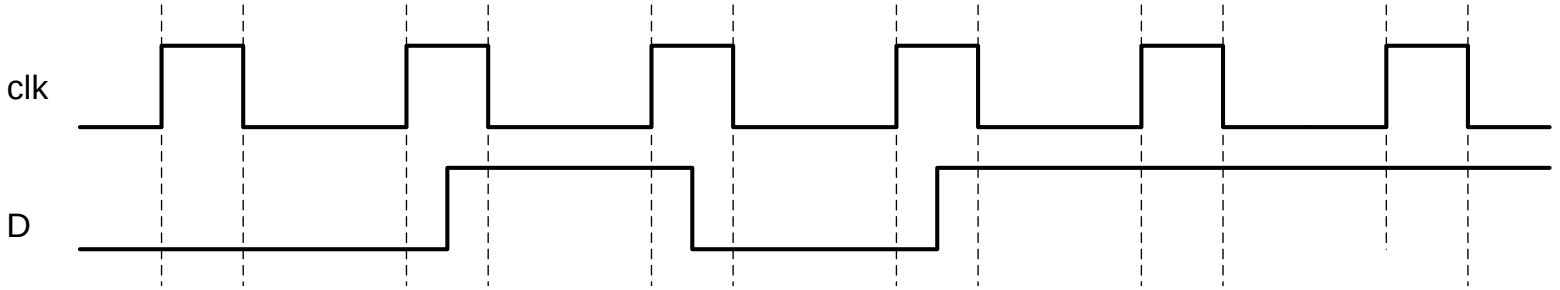


Negative edge triggered

D	clk	Q	$\overline{Q}$
0	↓	0	1
1	↓	1	0
x	↑	Q	$\overline{Q}$
x	0	Q	$\overline{Q}$
x	1	Q	$\overline{Q}$

Flip-flop (cont.)

- Draw the output waveform for the positive and negative edge triggered D flip-flops

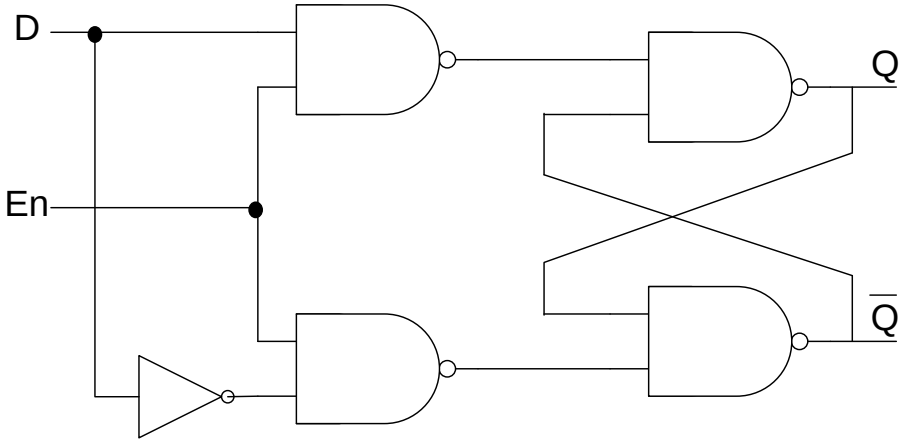


Q (+ve Flip-flop)

Q (-ve Flip-flop)

Flip-Flop (cont.)

- How to design flip-flops?
- Recall the Gated D Latch



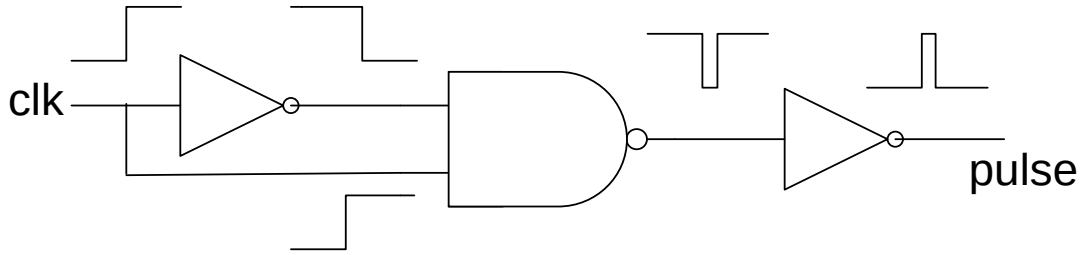
For Gated D Latch,
Q <= D when En = 1

For D Flip-flop,
Q <= D when En = ↑

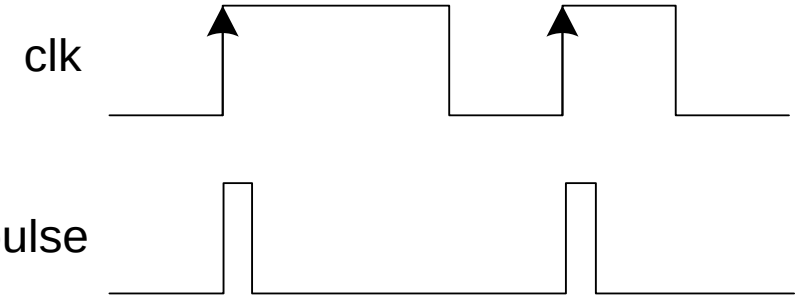
We need a pulse transition detector for a D Flip-flop, in order To detect ↑

Flip-Flop (cont.)

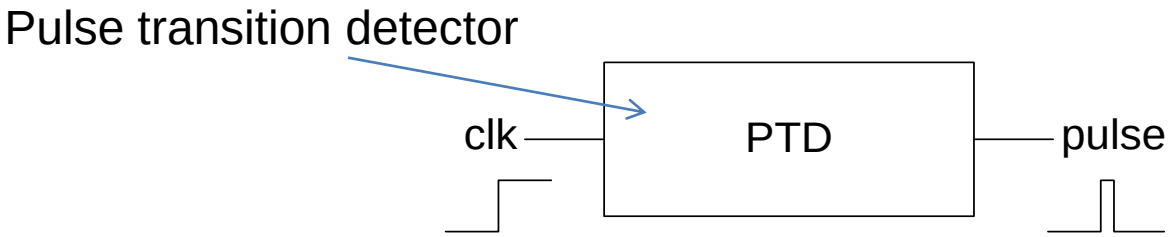
- Pulse transition detector



Circuit diagram

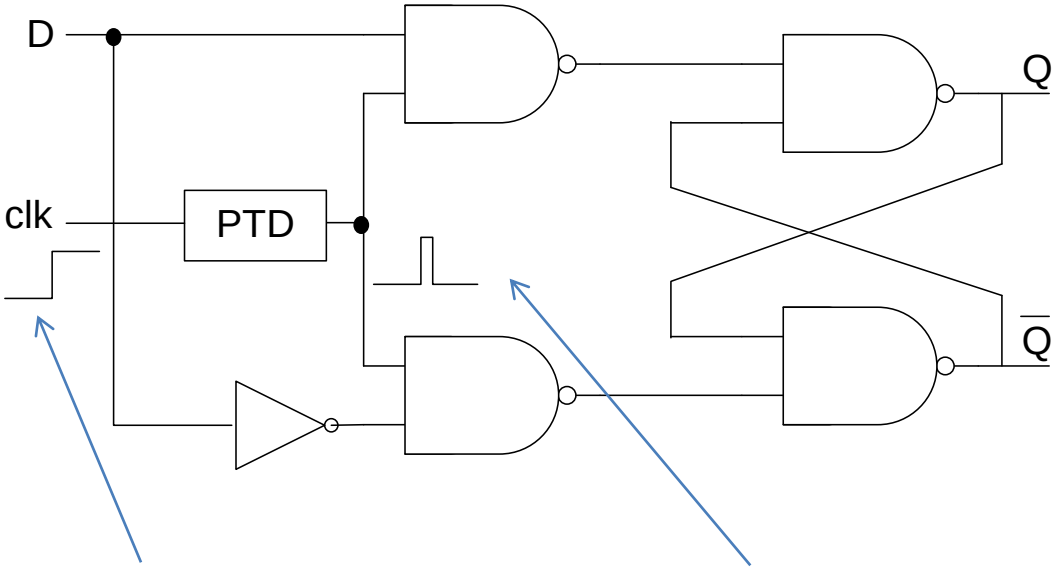


Waveform



Block diagram

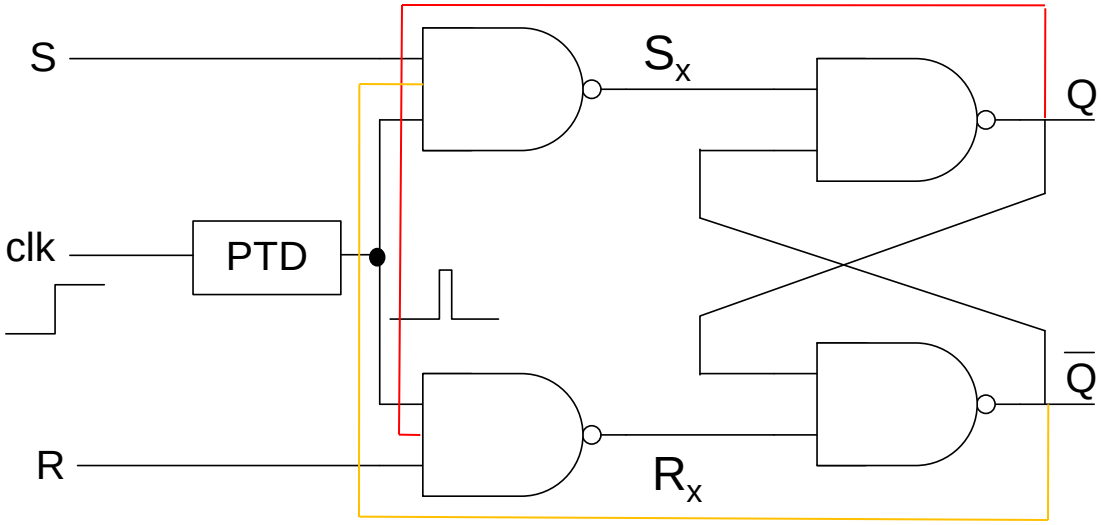
D Flip-flop



A positive edge of clk results in a short pulse at output of PTD, therefore, causes Q <= D only at that instant (pulse duration)
Q is maintained until the next positive edge of clk

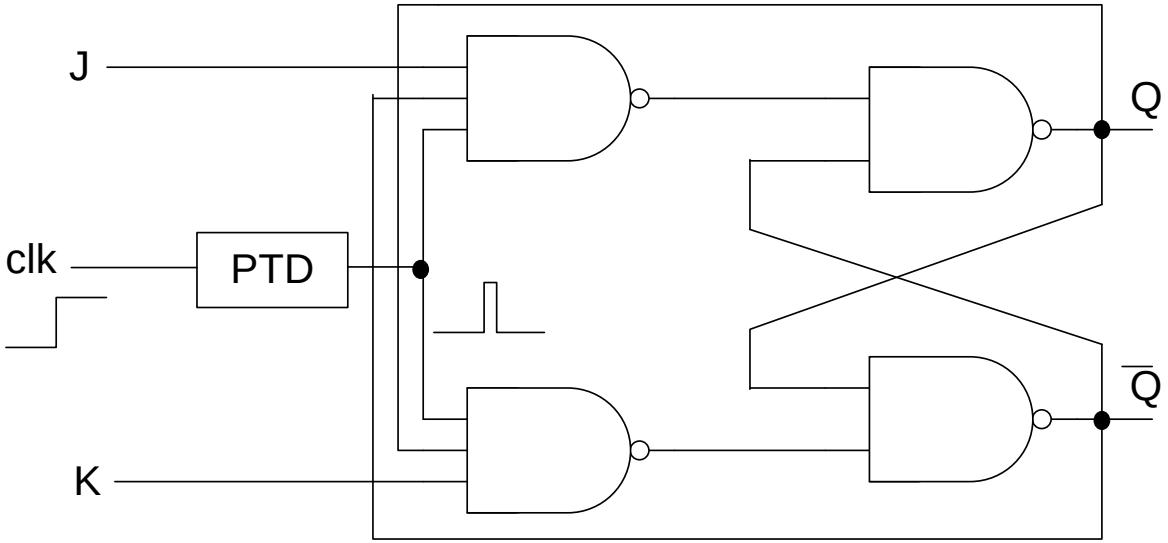
SR Flip-flop

- Recall the problem with SR Flip-flop



When S = 1 and R = 1, the outputs are invalid (both Q and $\overline{Q}$ equal to 1)
To overcome this problem, Q and $\overline{Q}$ is fed back to the Gated NANDs which now becomes the JK Flip-flop
S_x and R_x can never be equal to 0 at same time

JK Flip-flop

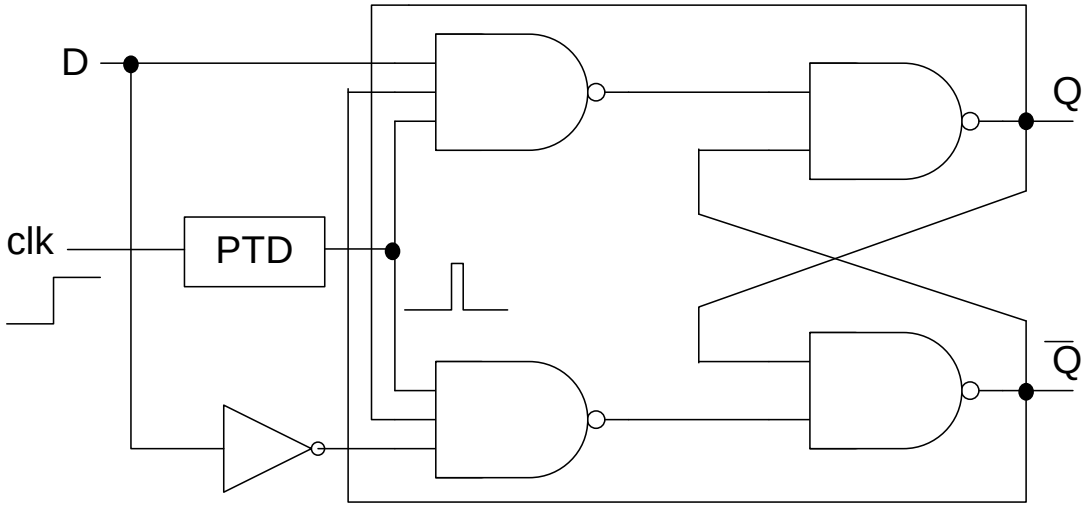


J	K	clk	Q	$\overline{Q}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
x	x	-	Q	$\overline{Q}$

When J = 1 and K = 1, Q and $\overline{Q}$ toggles
When J = 0 and K = 0, Q and Q maintains
When J = 0 and K = 1, Q = 0 (Reset)
When J = 1 and K = 0, Q = 1 (Set)

D Flip-flop

- We can also construct a D Flip-flop from JK Flip-flop by shorting J and K with an inverter

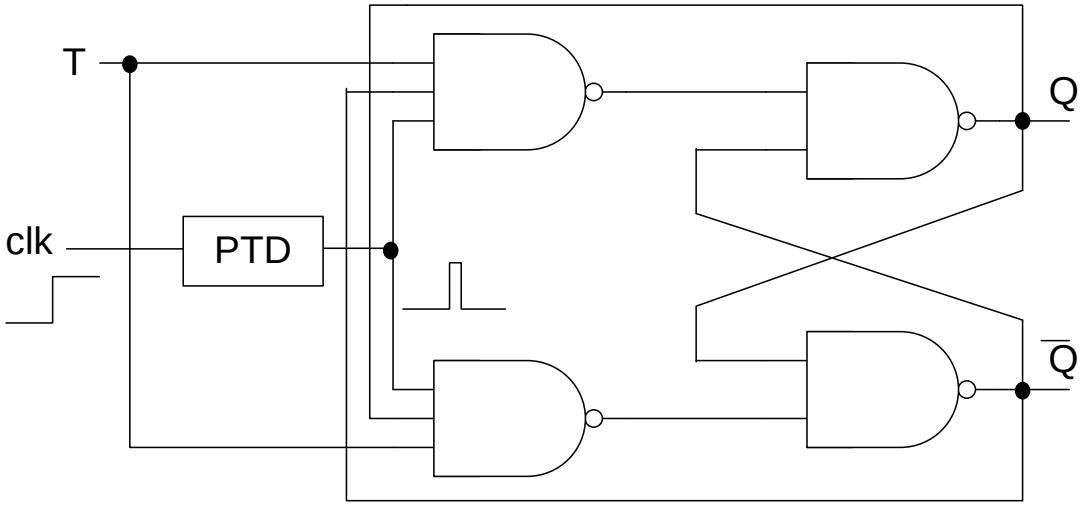


D clk	Q	$\overline{Q}$
0 ↑	0	1
1 ↑	1	0
x -	Q	$\overline{Q}$

Q <= D when clk = ↑
Else Q <= Q

T Flip-flop

- Another type of flip-flop, the T Flip-flop can be constructed from the JK flip flop by shorting J and K inputs

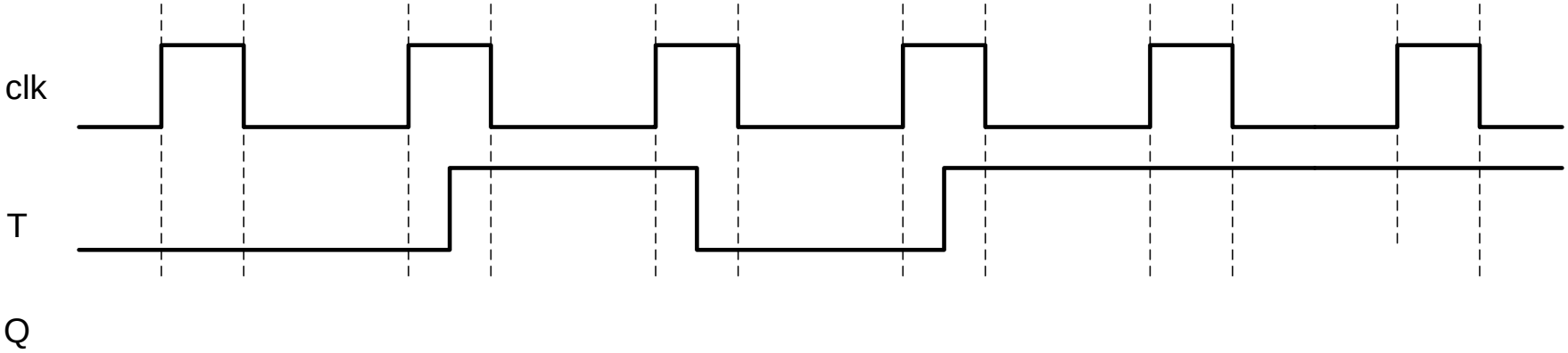


T clk	Q	$\overline{Q}$
0 ↑	Q	$\overline{Q}$
1 ↑	$\overline{Q}$	Q
x -	Q	$\overline{Q}$

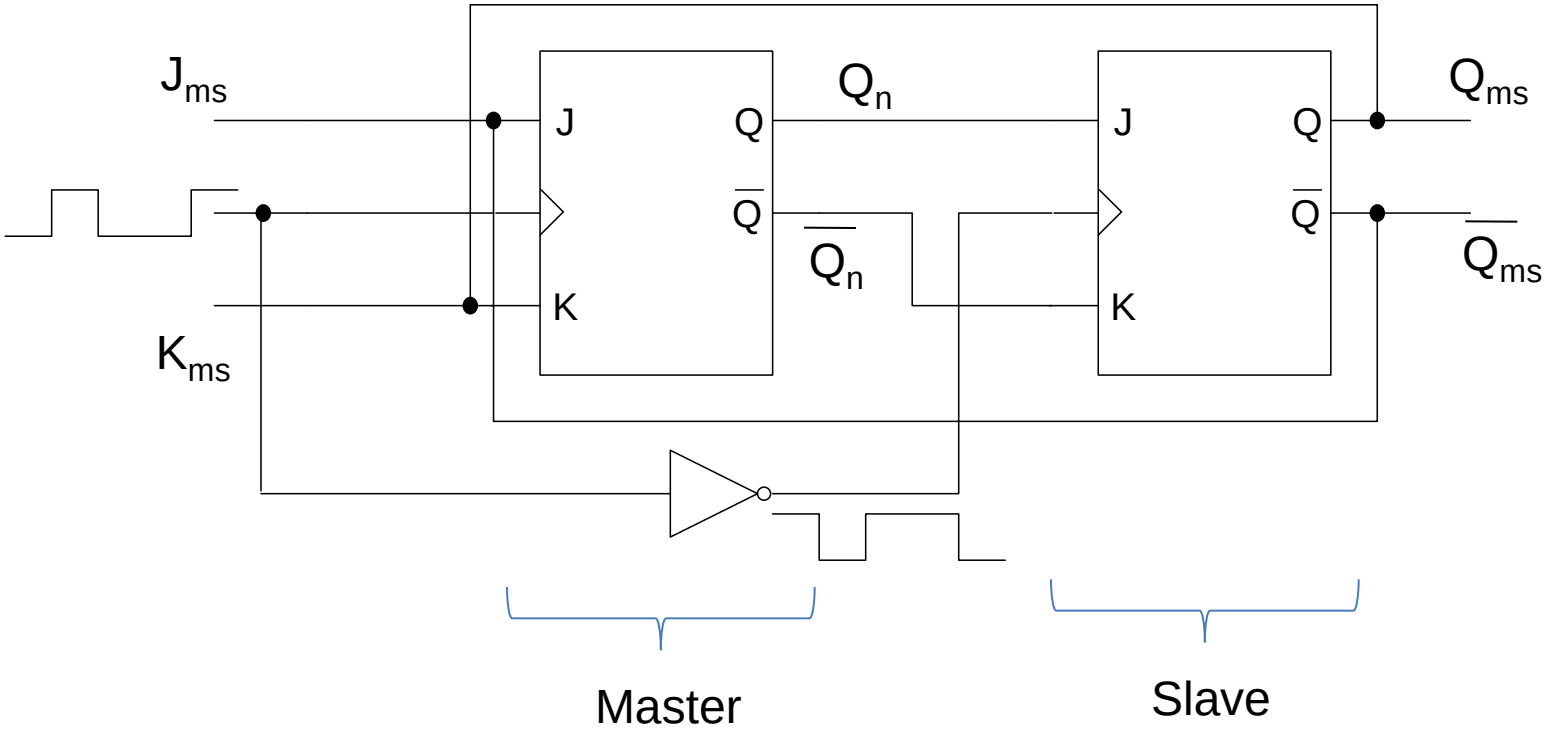
$Q <= \overline{Q}$ when T = 1 and clk = ↑
Else Q <= Q

T Flip-flop (cont.)

- Draw the output waveform for the positive edge triggered T Flip-flop



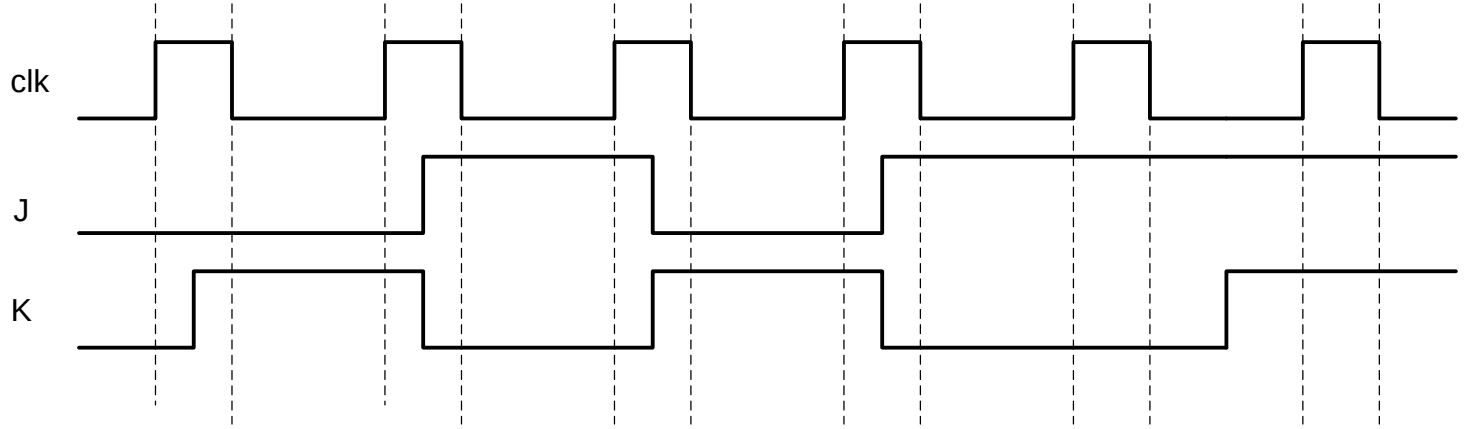
JK Master Slave Flip-Flop



Master latches data at positive edge of clk
Slave latches data at negative edge of clk
Q_{ms} is therefore valid on the negative edge of clk

JK Master Slave Flip-flop (cont.)

- Draw the output for JK Flip-flop and the JK Master Slave Flip-flop (MS-JK)

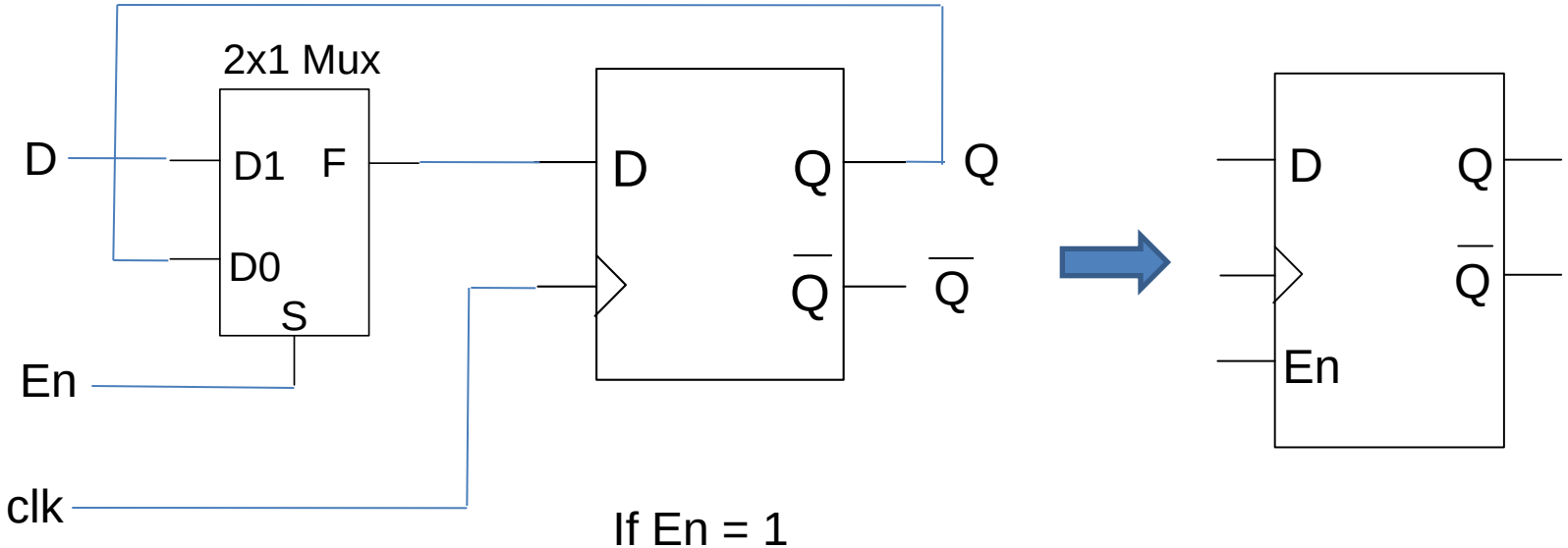


Q (JK Flip-flop)

Q (MS-JK Flip-flop)

Flip-flop Extra Features

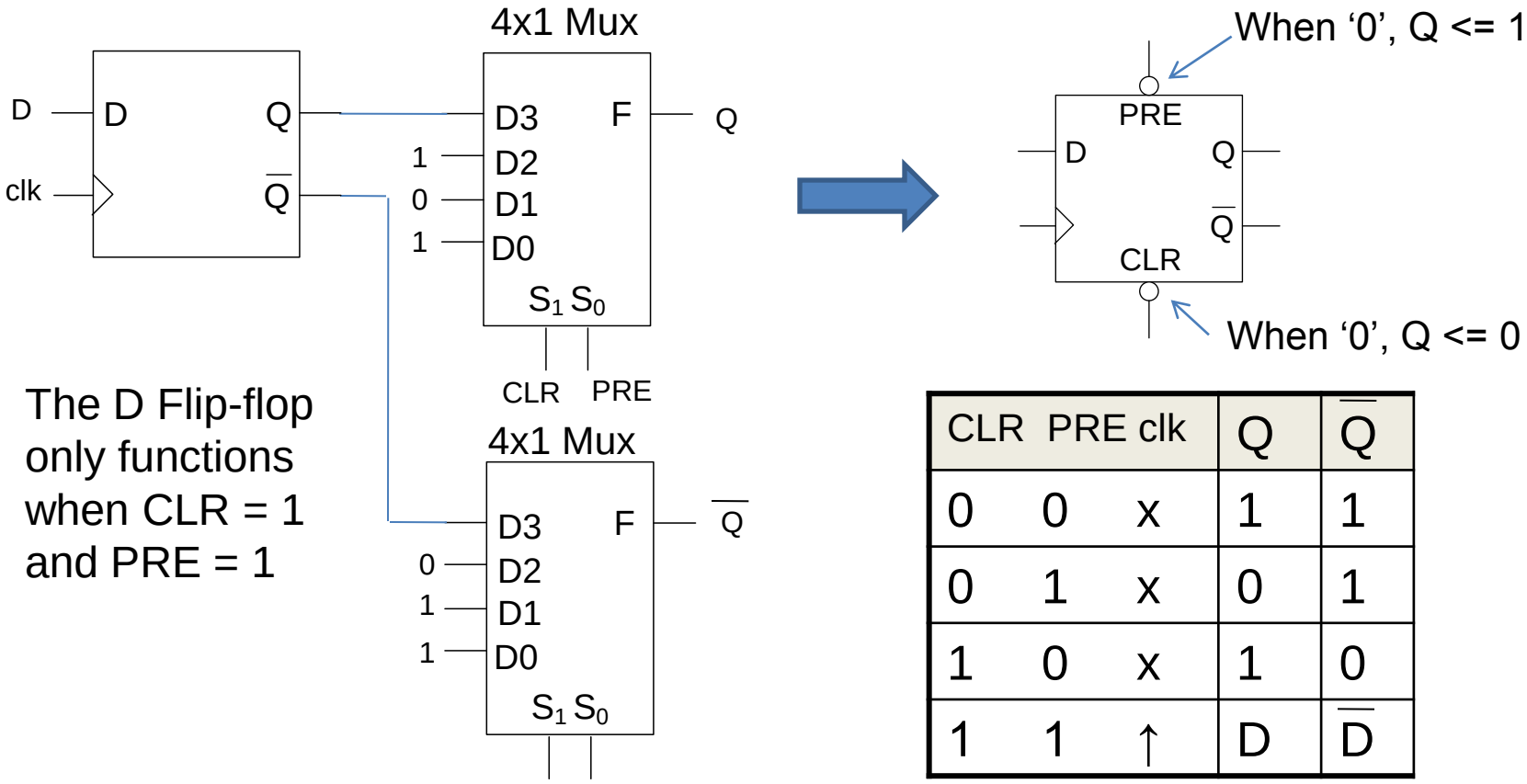
- Positive edge triggered D Flip-flop with active high Input Enable



If En = 1
    Q <= D when clk = ↑
Else
    Q <= Q

Flip-flop Extra Features (cont.)

- Positive Edge Triggered D Flip-flop with active low clear and active low preset functions

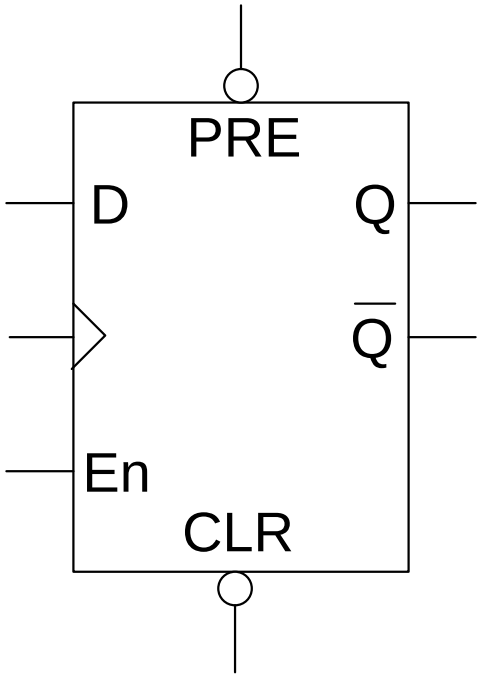


The D Flip-flop only functions when CLR = 1 and PRE = 1

CLR	PRE	clk	Q	$\overline{Q}$
0	0	x	1	1
0	1	x	0	1
1	0	x	1	0
1	1	↑	D	$\overline{D}$

Flip-flop Extra Features (cont.)

- Putting all together – Positive Edge Triggered D Flip-flop with active high enable, active low preset and active low clear



What is the input condition that Q <= D?
En = 1, clk = ↑, CLR = 1, PRE = 1

How to force Q <= 1?
En = x, clk = x, CLR = 1, PRE = 0

How to force Q <= 0?
En = x, clk = x, CLR = 0, PRE = 1

How to set Q <= Q at positive edge of clk?
En = 0, clk = ↑, CLR = 1, PRE = 1

Flip-flop IC

- The 7474 Dual Positive Edge Triggered D Flip-flop with preset, clear, and complementary outputs
- The 7476 Dual Master-Slave JK Flip-flops with clear, preset and complementary outputs